Amendments to the Drawings:

The attached replacement sheets of drawings, replacements for originally filed sheets 3/5 and 5/5, include changes to Figs. 5 and 9. The reference character "7", in Fig. 5, has been changed to "8" to comport with the description in the specification. The reference characters "81", "82" & "83" have been added to Fig. 9, to comport with their description in the specification. Applicants respectfully assert that the changes to the drawings render the objections thereto moot and Applicants respectfully request withdrawal of the objections to the drawings.

Attachments: Replacement Sheets 3/5 & 5/5

REMARKS

The Office Action dated August 11, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-32 are currently pending in the application. Claims 1-32 are respectfully resubmitted for consideration.

Claims 1-9, 14-22 and 27-32 were rejected under 35 U.S.C. §102(a) as being anticipated by *LEVEL ONE* (Level One™ IXP1200 Network Processor). Claims 10, 11, 23, 24 and 26 were rejected under 35 U.S.C. §103(a) as being unpatentable over *LEVEL ONE* in view of *Hegde* (U.S. Patent No. 6,570,875). Claims 12 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over *LEVEL ONE* in view of *Bray et al.* (U.S. Patent No. 6,483,849). The above rejections are respectfully traversed according to the remarks that follow.

The present invention is directed to, according to claim 1, from which claims 2-13 depend, a network switch for network communications. The network switch includes a first data port interface, the first data port interface supporting at least one data port transmitting and receiving data, a second data port interface, the second data port interface supporting at least one data port transmitting and receiving data, a CPU interface, the CPU interface configured to communicate with a CPU, a common memory, the common memory communicating with the first data port interface and the second data port interface, a memory management unit, the memory management unit for communicating data from the first data port interface and the second data port interface

and the common memory and at least two sets of communication channels, with each of the communication channels communicating data and messaging information between the first data port interface, the second data port interface, and the memory management unit. One set of communication channels of at least two sets of communication channels provides communication from the first and second data port interfaces to the memory management unit and another set of communication channels of at least two sets of communication channels provides communication from the memory management unit to the first and second data port interfaces.

The present invention is directed to, according to claim 14, from which claims 15-26 depend, a network switch for network communications. The network switch includes first data means providing a first data port interface supporting at least one data port transmitting and receiving data, second data means providing a second data port interface supporting at least one data port transmitting and receiving data, interface means providing an interface configured to communicate with a CPU, means for storing data, the means for storing data communicating with the first data means and the second data means, means for managing memory, the means for managing memory communicating data from the first data means and the second data means and the means for storing data and at least two sets of communication channel means, with each of the communication channel means communicating data and messaging information between the first data means, the second data means, and the means for managing memory. One set of communication channel means of at least two sets of communication channel means

provides communication from the first and second data means to the means for managing memory and another set of communication channel means of at least two sets of communication channel means provides communication from the means for managing memory to the first and second data means.

The present invention is directed to, according to claim 27, from which claims 28-32 depend, a method of handling data packets in a network switch. The method includes the steps of receiving at a data port an incoming data packet, resolving a destination address of the incoming data packet, discarding, forwarding, or modifying the packet based upon the resolving step, placing at least a portion of the data packet on a first communication channel, when the packet is to be forwarded, receiving at the data port a section of another data packet on a second communication channel from a common memory and forwarding the another data packet from the data port, where the first and second channels are separate from each other.

As discussed in the present specification, the present invention provides a network device that utilizes two separate sets of communications channels, such that one channel ferries data from ports of the switch to memory and the other channel ferries data from the memory to the ports. It is respectfully submitted that the prior art of *LEVEL ONE*, *Hegde* and *Bray et al.*, taken together or separately, fail to disclose or suggest all of the elements of any of the presently pending claims. Therefore, the prior art fails to provide the critical and unobvious advantages discussed above.

LEVEL ONE is directed to a network processor that is used to switch data on a network. The Office Action points to Figure 1 of *LEVEL ONE* as teachings multiple data port interfaces, a CPU interface, common memory, a MMU and "at least two set [sic] of communication channels for communicating data and messaging information." The rejection appears to acknowledge that claims 1, 14 and 27 recite a set of channels to move data and messages from the port interfaces to the MMU and another set to move data and messages to the port interfaces from the MMU, but alleges that such elements can be found in the bi-directional nature of the bus. However, Applicants respectfully assert that *LEVEL ONE* fails to teach or suggest all of the elements of claims 1, 14 and 27.

Claims 1, 14 and 27 recite, in part, first and second data port interfaces, "supporting at least one data port transmitting and receiving data" and "at least two sets of communication channels." Looking to Figure 1 of *LEVEL ONE* and its associated description, it would appear that the "10/100/1Gb Ethernet MAC" and the "ATM, T1/E1, Other MAC" could be equivalent to data port interfaces. However, both of those interface modules are illustrated as being serviced by a single "FIFO Bas 66 MHz," and does not illustrated two sets of channels. A review of the description of the FIFO bus make it clear that it does not teach or suggest the presence of at least two sets of channels being encompassed by that bus. Thus, Applicants respectfully assert that at least the element of "at least two sets of communication channels" in claims 1, 14 and 27 is neither taught nor suggested.

It could also be argued, although it is not clear that the Office Action does so, that the illustrated "PCI Bus 66 MHz" would constitute another set of communications channels. However, such a position would not be tenable because the elements illustrated as being serviced by the PCI bus would be the optional host CPU and PCI MAC devices. As those latter elements are described in the reference, it is clear that they could not be thought of as "data port interfaces" which support at least one data port transmitting and receiving data. Additionally, even with the presence of the second bus, it would not have been obvious to modify the "sets of communication channels" such that a set of channels that moves data and messages from the port interfaces to the MMU and another set that moves data and messages to the port interfaces from the MMU. Since one bus is a PCI bus and the other is a FIFO bus, data port interfaces would not be supported by the PCI bus. As such, Applicants respectfully assert that all of the elements of claims 1, 14 and 27 are neither taught nor suggested by *LEVEL ONE*. Thus, Applicants respectfully assert that the rejection is improper and should be withdrawn.

With respect to the rejections of claims 10-13 and 23-26, the Office Action acknowledges that *LEVEL ONE* fails to teach or suggest all of the elements of those claims. Because of this, the Office Action also cites *Hegde* and *Bray et al.* in the alleged rejections of those claims. *Hegde* is cited for its alleged teachings of the use of a VLAN table and *Bray et al.* is cited for its alleged teachings of auto-negotiation. However, even if the latter references were accepted for what they are alleged to teach, they would not cure the deficiencies of *LEVEL ONE* noted above. As such, Applicants respectfully

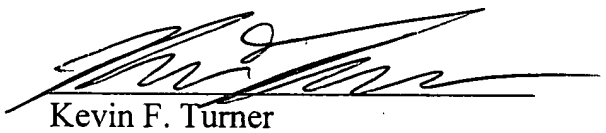
traverse the rejection of claims 10-13 and 23-26 for at least their dependence on claims 1 and 14.

In view of the above, Applicants respectfully submit that claims 1-32 each recite subject matter which is neither disclosed nor suggested by *LEVEL ONE*, *Hegde* and *Bray et al.* It is therefore respectfully requested that all of claims 1-32 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Kevin F. Turner
Registration No. 43,437

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7856
Fax: 703-720-7802

KFT:noe:tdg